REMARKS

Applicants respectfully traverse and request reconsideration. Applicants would again like to thank the Examiner for allowing claim 40 and for indicating that claims 7 through 12, 14, 16 and 17 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Objections

On page 2 of the Office Action (reference no. 1), the drawings are objected to because, according to the Office Action, "Claim 41's last limitation which states that the selector circuit is operatively coupled to [cause the] input buffer to provide the first internal signal from the first internal signal path must be shown or the feature(s) cancelled from the claim(s)." Support for this language may be found at least in Figure 5 and in the specification on page 16, lines 8 through 10 (the output buffer 164 of the pair of buffers passes bus bridge signals from the internal bus bridge data-out flip-flop 102 via the AGP bus 190 (shown in FIG. 4) to the external circuit 150). As explained in the specification, the output buffer 164 passes bus bridge signals from the internal bus bridge data-out flip-flop 102 via the AGP bus 190. Further, Figure 5 illustrates the output buffer 164 with the bufferless data path 122 as an input and the AGP bus extension 192 as an output according to one embodiment and thus supports claim 41. Accordingly, in view of the above reasons, the objection is improper and withdrawal of the above rejection is requested.

Claim Rejections under 35 U.S.C. § 112

The Office Action rejects Claims 41 through 43 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. According to the Office Action, "Claim 41's last limitation which states that the selector circuit is operatively coupled to the input buffer to provide the first internal signal from the first internal signal path to the first external signal path is not in the written description." As stated above, the specification on page 16, lines 8 through 10 and Figures 4 and 5 provide adequate support for the cited language in claim 41. The comments from the previous responses are also repeated. Accordingly, in view of the above reasons, the rejection is improper and withdrawal of the above rejection is requested.

Claims 21 through 23 and 25 through 27

Claims 21 through 23 and 25 through 27 are rejected under 35 U.S.C. § 102(e) as being anticipated by Melo, et al. ("Melo") (U.S. Patent No. 6,040,845). Claim 1 is rejected entirely based on Figure 1 of Melo.

According to the Office Action, Melo discloses a south bridge 28 in Figure 1 for arbitrating and controlling the signals from any external circuit (I/O 32a, 302b) from reaching the internal circuit and thus prevents signals from the external circuits I/O 32a, 302b from reaching the south bridge 28. However, Melo teaches arbitration with respect to the AGP bus between north bridge 14 and the graphics accelerator 20 rather between than the peripheral bus between the south bridge 28 and the I/O circuits 32a, 302b. (Abstract line 5; Col. 5, lines 23–35.) Melo teaches providing connectivity between the south bridge 28 and the I/O devices 32a, 302b such as via a peripheral bus. (Melo, Col. 5, lines 3–8.) Melo seeks to reduce power consumption by powering off the graphics circuit when arbitration determines the graphics circuit is not requested. (Melo, Col. 2, lines 45–67.) Further, even if Melo did teach arbitration bus communication between the south bridge 28 and the I/O devices 32a, 302b, arbiter 44 merely grants mastership to the bus and does not prevent signals from the I/O devices 32a, 302b from reaching the internal circuit. (Melo, Col. 5, lines 23–28.) Melo teaches granting mastership of the AGP bus between two different types of masters: the graphics master 46 or a peripheral master (PCI master) 48 in the north bridge 13. (Melo, Col. 5, lines 26–28.) The device that is not the master "suspends pipelined data transfer and using the grant signal, allows the bus master to initiate a bus transaction." (Melo, Col. 6, line 40.) Therefore, merely suspending pipelined data transfer allows the bus master to initiate a bus transaction, thereby permitting signals to reach the device that is not the master. As a result, the device that is not the master must receive the signals from the master.

In contrast, the claims teach "at an internal I/O circuit, preventing signals from any external circuit from reaching the internal circuit" rather than allowing signals from reaching the internal circuit while arbitrating access to a common AGP bus as taught in Melo. Further, the Melo reference suffers from the same problems as described in Applicants' "Background of the Invention." Signals propagate along the common bus in a conventional bus architecture. (Specification, page 3, lines 9–21.) Since signals propagate through the common bus between the graphics controller and the bus bridge, signal reflections occur on the bus, thereby causing

data errors and limiting the bus clock speed. (Specification, page 3, line 22–page 4, line 4.) Therefore, by preventing signals from reaching the internal circuit, signal reflections may be reduced. (Specification, page 4, lines 24–30.)

As a result, since Melo explicitly teaches arbitrating communication of signals across a conventional bus to the external circuit and the internal I/O circuit, Melo necessarily fails to teach and further teaches away from, among other things, "preventing signals from any external circuit from reaching the internal circuit." Consequently, Melo fails to teach all the elements as arranged in claim 21, namely, "at an internal circuit, receiving a bus bridge signal from an internal bus bridge; and at an internal I/O circuit, preventing signals from any external circuit from reaching the internal circuit." Therefore, Melo fails to teach all the elements as arranged in claim 21 and as a result Melo does not anticipate claim 21.

As to claim 22, the Office Action merely relies on Figure 2 of Melo to reject the elements of claim 22. According to the Office Action, the external circuit is equated to the graphics master peripheral target 46 and receives the bus bridge signal from the internal bus bridge, and the external circuit 46 reflects the bus bridge signal to the internal I/O circuit (equated to structure 40). However, in contradictory fashion, in the rejection to claim 21, the external circuit was equated to I/O circuits 32a, 302b and the internal I/O circuit was equated to south bridge 28. Nevertheless, Applicants repeat the relevant remarks made above, including those indicating that the signals on the AGP bus are sent between the external circuit 46 and structure 40. As a result, Melo necessarily fails to teach and further teaches away from, among other things, "preventing signals from any external circuit from reaching the internal circuit." Additionally, claim 22 includes new and nonobvious subject matter and is also believed to be in condition for allowance.

Claims 21 through 23, 25 through 27, 29 through 33 and 35 through 38 are rejected under 35 U.S.C. § 102(e) as being anticipated by Bickford et al. ("Bickford") (U.S. Patent No. 6,141,021).

As to Claim 21, Bickford is directed to a video system 100 including an accelerator graphics port (AGP) bus 110 coupled to an AGP graphics accelerator chip 118 and an AGP graphics accelerator add-in card 122. (Bickford ¶ 4, lines 33–49.) A disable device 124 selectively disables either the video down AGP graphics accelerator 118 or the add-in AGP card 122 for avoiding bus contention on an accelerator graphics port (AGP). (Bickford ¶ 4, lines 46–49.) Thus, two AGP accelerators 118, 122 may be *simultaneously coupled to the AGP 110,* since

the disabled device 124 disables one of the AGP graphics accelerators 118, 122 and prevents both devices 118, 122 from contending for the AGP 110. (Bickford ¶ 4, lines 49–53.) Bickford teaches resolving a completely different problem from that of the claims. For example, Bickford seeks to solve the problem of resolving bus contention, whereas the claims recite "at an internal I/O circuit, preventing signals from any external circuit from reaching the internal circuit." Further, Bickford suffers from the same problems as described in Applicants' "Background of the Invention" as stated above with respect to Bickford. Consequently, Bickford fails to teach all the elements as arranged in claim 21 and as a result Bickford does not anticipate claim 21.

As to claim 23, Applicants respectfully reassert the relevant remarks made above. Further, claim 23 includes new and nonobvious subject matter and is also believed to be in condition for allowance.

As to claims 26, 27, 30 through 33, 35, 37 and 38, Applicants respectfully reassert the relevant remarks made above. Further, these claims add new and nonobvious subject matter and are believed to be in condition for allowance.

As to claim 29, Applicants respectfully reassert the relevant remarks made above with respect to claim 21 and note that Bickford does not teach, among other things, an integrated bus bridge graphics unit coupled to memory that includes an internal circuit operably configured to avoid signals from an external graphics bus. Instead, Bickford, as previously stated, teaches enabling and disabling the AGP graphics accelerators. Since Bickford teaches that the internal graphics bus is coupled directly to the external slot and to the internal AGP graphics chip (see Figure 3), no external graphics path or bus is taught by Bickford. Bickford simply controls the receipt of a frame # signal from the PCI bus to either of the two graphics controllers to enable or disable one of the two graphics controllers. Further, this claim includes new and nonobvious subject matter and is also believed to be in condition for allowance. Consequently, Bickford fails to anticipate claim 29.

Claim Rejections under 35 U.S.C. § 103

Claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,621,900 (Lane) in view of U.S. Patent No. 5,633,599 (Kubota) or U.S. Patent No. 5,850,530 (Chen).

The Office Action acknowledges that Lane does not explicitly disclose an input buffer for the bridge. The Office Action fails to show how the selector circuit, equated to host bus bridge

107, is described as operable to select either the first internal signal or the first external signal. In contrast to the assertion in the Office Action as shown above, the selector circuit, equated to 107 in Figure 1 of Lane, bridges bus transactions (Lane, Col. 3, lines 44–49) and therefore performs no selection of signals as arranged in the claims. Further, the Office Action fails to explain why or where Lane states that the computer bus suffers from any *retry* problems, especially within a computer. Consequently, one would not be motivated to modify Lane to add the input buffer as asserted. Therefore, the combination of the references fail to establish a prima facie case of obviousness. As a result, the rejection of claim 1 is improper.

Claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Melo in view of Kubota or Chen. Applicants repeat the relevant remarks above. The Office Action acknowledges that Melo does not disclose an input buffer. The Office Action fails to show where Melo teaches the selector circuit described as operable to select either the first internal signal or the first external signal. Nevertheless, as state above, Melo teaches arbitration to allocate mastership within the AGP bus. Therefore, the combination of Melo, Kubota or Chen fails to describe each and every element in claim 1. As a result, one would not be motivated to modify Melo to add the input buffer as asserted. Therefore, despite the assertion in the Office Action, fails to establish a prima facie case of obviousness. As a result, the rejection of claim 1 is improper.

Claims 1 through 5, 13, 15, 18 through 20, 24, 34 and 41 through 43 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bickford in view of Kubota or Chen. Applicants repeat the relevant remarks above. The Office Action acknowledges that Bickford does not disclose an input buffer. Further, since Bickford teaches disable device 124 to disable either the AGP accelerator 118 or the add-in card 122 and thus perform bus selection, modifying Bickford to add an input buffer would be redundant and therefore unnecessary. Therefore, one would not be motivated to modify Bickford to add the input buffer as asserted. Consequently, the combination of the references fails to establish a prima facie case of obviousness. As a result, the rejection of claim 1 is improper.

With regard to Claim 2, the Office Action admits that Bickford does not disclose, among other things, a separate second internal signal path for conveying its signal to the output buffer. The Office Action, however, alleges that duplication of working parts of the device which are normally formed in two pieces is well known and that only routine skill in the computer art would be needed to add an additional internal signal path and to integrate the external output

path and external input path into one external path. Applicants challenge that such a two-piece system would be needed when such a modification would make the arbiter circuit redundant.

Bickford also fails to describe the output buffer as operative to receive a second internal signal via the second internal path and to provide the second internal signal via the first external signal path as recited in claim 2. Accordingly, such a combination of the internal circuit, input buffer, output buffer and selector circuit is not taught or suggested by the cited references. Further, as stated above, the references teach away from such a combination as claimed. The Applicants hereby incorporate the previous arguments made in all prior Office Action Responses, including those arguments relating to Bickford teaching away from the claims, and on those grounds the Applicants respectfully submit that the Office Action fails to show motivation for one to combine the references as asserted by the Office Action. Further, the Applicants repeat the above relevant remarks and in addition have shown that Bickford teaches away from the claims and one would not be motivated to modify Bickford with Kubota and Chen. Consequently, the Office Action fails to establish a prima facie case of obviousness. Applicants repeat the relevant comments made above.

As to claims 3, 4, 5, 13, 15, 18 through 20, 24, 34 and 41 through 43, Applicants respectfully reassert the relevant remarks made above and again note that these claims add new and nonobvious subject matter. As a result, these claims are believed to be in condition for allowance.

With regard to dependent claims 6, 28, 39 and 34, Applicants respectfully reassert the relevant remarks made above with respect to the above claims. For at least the reasons stated above, the Office Action fails to establish a prima facie case of obviousness for claims 6, 28 and 39. Further, claims 6, 28 and 39 include new and nonobvious subject matter and are believed to be in condition for allowance.

Accordingly, Applicant respectfully submits that the Claims are in condition for allowance and requests that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

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Respectfully submitted,

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